

DS26LS31C, DS26LS31M

SNOSBK1C-JUNE 1998-REVISED APRIL 2013

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

Check for Samples: DS26LS31C, DS26LS31M

FEATURES

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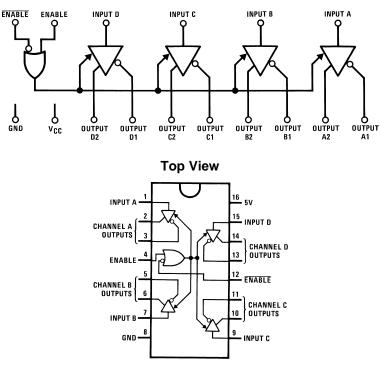
- Output Skew—2.0 ns Typical
- Input to output delay—10 ns Typical
- Operation from Single 5V Supply
- Outputs Won't Load Line when V_{CC} = 0V
- Four Line Drivers in One Package for Maximum Package Density
- Output Short-Circuit Protection
- Complementary Outputs
- Meets the Requirements of EIA Standard RS-422
- Pin Compatible with AM26LS31
- Available in Military and Commercial Temperature Range

Logic and Connection Diagrams

DESCRIPTION

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. PDIP Package See Package D0016A or NFG0016E See Package Numbers NAJ0020A, NFE0016A or NAD0016A

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

7V
7V
5.5V
-0.25 to 6V
1509 mW
1476 mW
1051 mW

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics provide conditions for actual device operation.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V _{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T _A			
DS26LS31M	-55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

	Parameter	Parameter Test Conditions				Units	
V _{OH}	Output High Voltage	I _{OH} = −20 mA	2.5			V	
V _{OL}	Output Low Voltage	I _{OL} = 20 mA			0.5	V	
VIH	Input High Voltage		2.0			V	
V _{IL}	Input Low Voltage				0.8	V	
IIL	Input Low Current	$V_{IN} = 0.4V$		-40	-200	μA	
I _{IH}	Input High Current	V _{IN} = 2.7V			20	μA	
I _I	Input Reverse Current	V _{IN} = 7V			0.1	mA	
l _o	TRI-STATE Output Current	$V_{O} = 2.5V$			20	μA	
		$V_{O} = 0.5V$			-20	μA	
V _{CL}	Input Clamp Voltage	I _{IN} = −18 mA			-1.5	V	
I _{SC}	Output Short-Circuit Current		-30		-150	mA	
I _{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA	

(1) Unless otherwise specified min/max limits apply across the -55° C to $+125^{\circ}$ C temperature range for the DS726LS31M and across the 0°C to $+70^{\circ}$ C range for the DS26LS31. All typicals are given for V _{CC} = 5V and T_A = 25^{\circ}C.

(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

(3) Only one output at a time should be shorted.

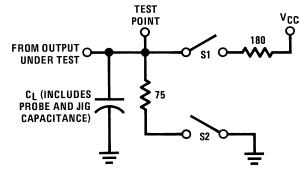
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Switching Characteristics

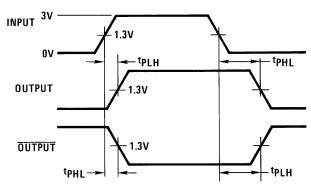
$V_{CC} = 5V, T_A = 25^{\circ}C$									
	Parameter	Test Conditions	Min	Тур	Max	Units			
t _{PLH}	Input to Output	C _L = 30 pF		10	15	ns			
t _{PHL}	Input to Output	C _L = 30 pF		10	15	ns			
Skew	Output to Output	C _L = 30 pF		2.0	6.0	ns			
t _{LZ}	Enable to Output	C _L = 10 pF, S2 Open		15	35	ns			
t _{HZ}	Enable to Output	C _L = 10 pF, S1 Open		15	25	ns			
t _{ZL}	Enable to Output	C _L = 30 pF, S2 Open		20	30	ns			
t _{ZH}	Enable to Output	C _L = 30 pF, S1 Open		20	30	ns			

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



S1 and S2 of load circuit are closed except where shown.

Figure 2. AC Test Circuit



 $f = 1 \text{ MHz}, t_r \le 15 \text{ ns}, t_f \le 6 \text{ ns}$

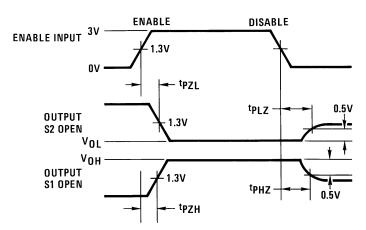


DS26LS31C, DS26LS31M

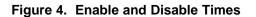


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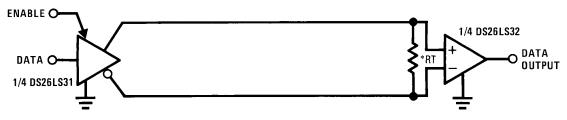
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 $f = 1 \text{ MHz}, t_r \le 15 \text{ ns}, t_f \le 6 \text{ ns}$



TYPICAL APPLICATIONS



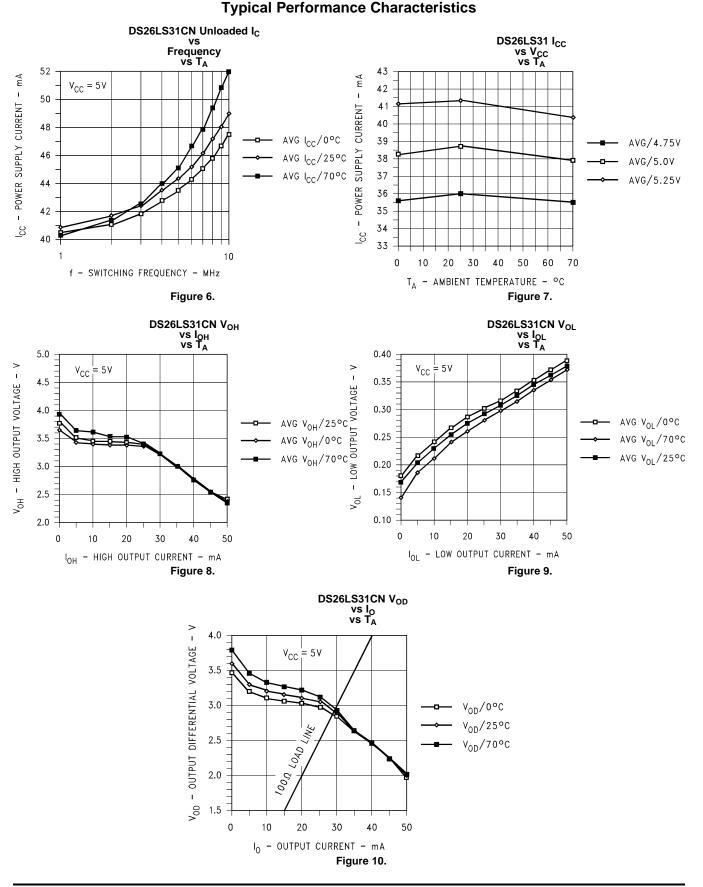
 R_T is optional although highly recommended to reduce reflection.





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REVISION HISTORY

Cł	nanges from Revision B (April 2013) to Revision C Pa	age
•	Changed layout of National Data Sheet to TI format	5



1-Nov-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
AM26LS31PC	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DS26LS31CN AM26LS31PC	
DS26LS31CM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DS26LS31CM	
DS26LS31CM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS31CM	Samples
DS26LS31CMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DS26LS31CM	
DS26LS31CMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS26LS31CM	Samples
DS26LS31CN	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DS26LS31CN AM26LS31PC	
DS26LS31CN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	CU SN	Level-1-NA-UNLIM	0 to 70	DS26LS31CN AM26LS31PC	Samples
DS26LS31N	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DS26LS31CN AM26LS31PC	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26LS31CMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26LS31CMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

18-Aug-2014

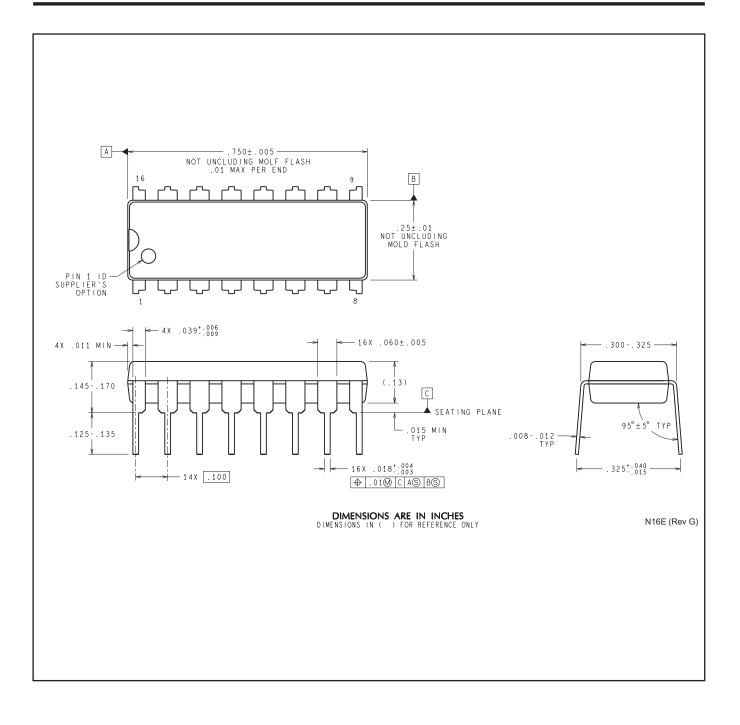


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26LS31CMX	SOIC	D	16	2500	367.0	367.0	35.0
DS26LS31CMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

MECHANICAL DATA

NFG0016E





D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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