HEF4526B

Programmable 4-bit binary down counter

Rev. 5 — 22 November 2011   **Product data sheet**

1. General description

The HEF4526B is a synchronous programmable 4-bit binary down counter with active HIGH and active LOW clock inputs (CP0, $\overline{CP1}$), an asynchronous parallel load input (PL), four parallel inputs (A0 to A3), a cascade feedback input (CF), four buffered parallel outputs (Q0 to Q3), a terminal count output (TC), an overriding asynchronous master reset input (MR) and a decoded TC output that can be used for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on A0 to A3 is loaded into the counter while PL is HIGH, independent of all other inputs except MR, which must be LOW. When PL and $\overline{CP1}$ are LOW, the counter advances on a LOW-to-HIGH transition of CP0. When PL is LOW and CP0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP1}$. TC is HIGH when the counter is in the zero state (Q0 = Q1 = Q2 = Q3 = LOW) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (Q0 to Q3 = LOW) independent of other inputs. The clock input is highly tolerant of slower clock rise and fall times due to Schmitt trigger action.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1.   Ordering information
All types operate from −40 °C to +85 °C.

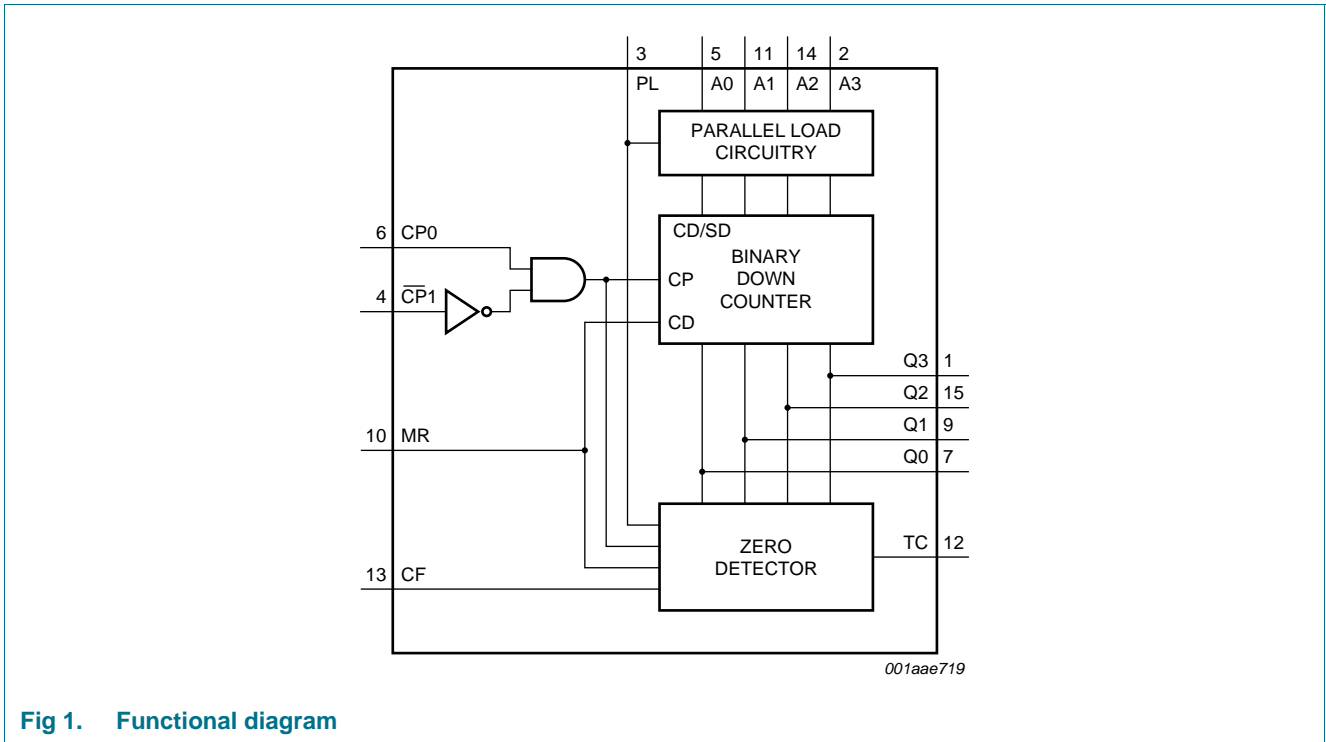| Type number	Package		
	Name	**Description**	**Version**
HEF4526BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4526BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4.   Functional diagram

Fig 1.   Functional diagram
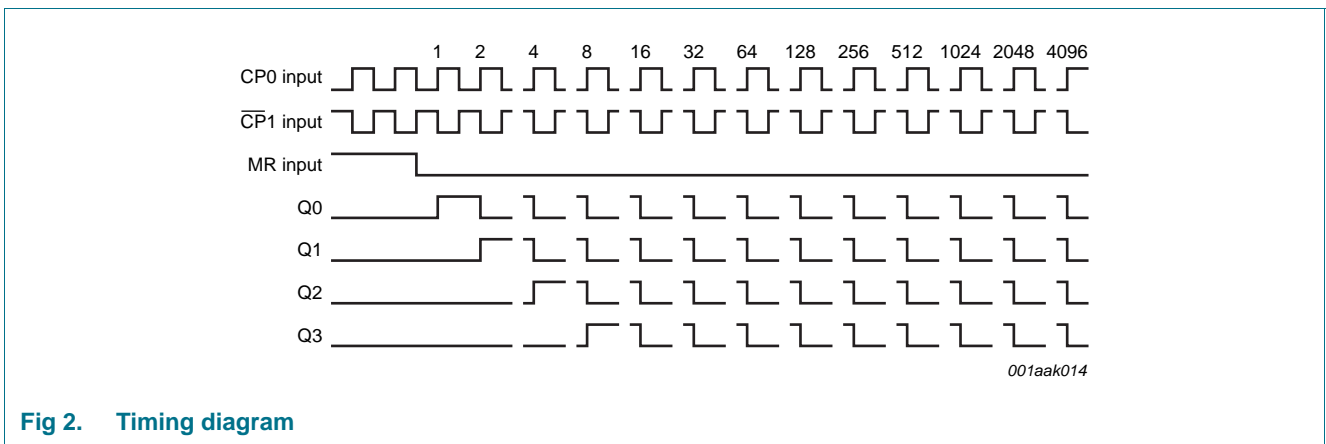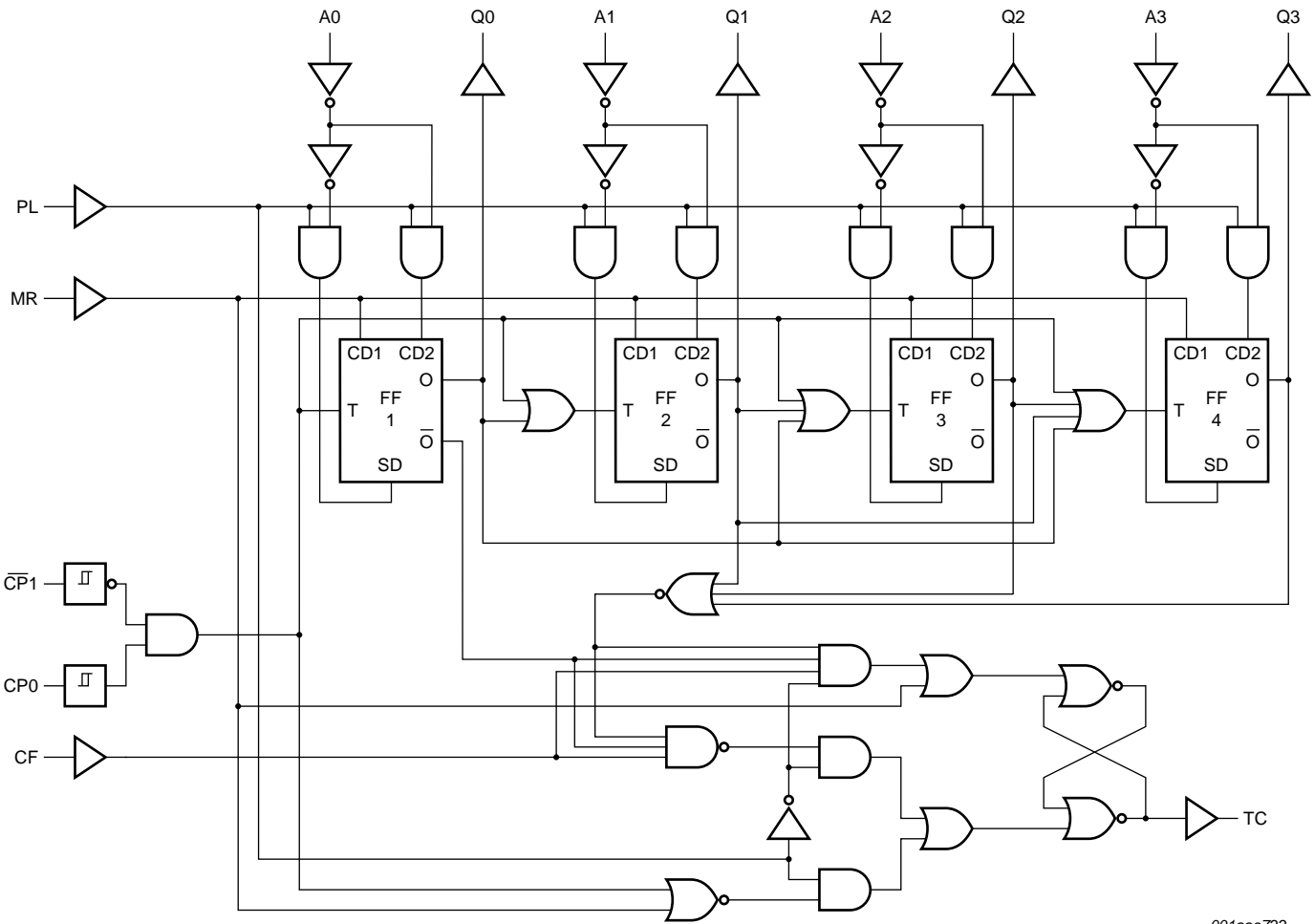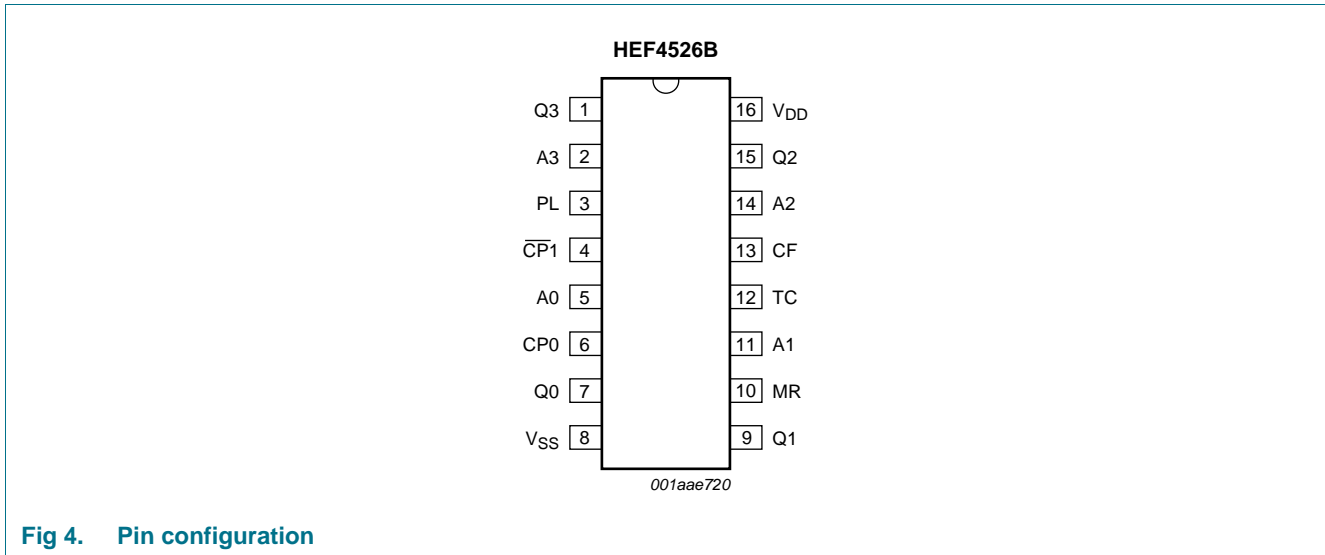

Fig 2.   Timing diagram

HEF4526B

Product data sheet

Rev. 5 — 22 November 2011

2 of 19

001aae722

Fig 3.   **Logic diagram**

5. Pinning information

5.1 Pinning

HEF4526B

Q3	1		16	V$_{DD}$
A3	2		15	Q2
PL	3		14	A2
$\overline{CP1}$	4		13	CF
A0	5		12	TC
CP0	6		11	A1
Q0	7		10	MR
V$_{SS}$	8		9	Q1

001aae720

Fig 4.   Pin configuration

5.2 Pin description

Table 2.   Pin description

Symbol	Pin	Description
A0 to A3	5, 11, 14, 2	parallel input
PL	3	parallel load input
CP0	6	clock input (LOW-to-HIGH, triggered)
$\overline{CP1}$	4	clock input (HIGH-to-LOW, triggered)
CF	13	cascade feedback input
MR	10	asynchronous master reset input
TC	12	terminal count output
Q0 to Q3	7, 9, 15, 1	buffered parallel output
V$_{DD}$	16	supply voltage
V$_{SS}$	8	ground (0 V)

HEF4526B

Product data sheet **Rev. 5 — 22 November 2011** 4 of 19

6. Functional description

Table 3.   Function table[1]

MR	PL	CP0	CP1	Mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	↑	H	no change
L	L	L	↓	no change
L	L	↓	X	no change
L	L	X	↑	no change
L	L	↑	L	counter advances
L	L	H	↓	counter advances

[1]   H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

Table 4.   Counting mode
CF = HIGH; PL = LOW; MR = LOW.

Count	Outputs			
	Q3	Q2	Q1	Q0
15	H	H	H	H
14	H	H	H	L
13	H	H	L	H
12	H	H	L	L
11	H	L	H	H
10	H	L	H	L
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

HEF4526B

Product data sheet **Rev. 5 — 22 November 2011** 5 of 19

Table 5. **Single stage operation**
Divide-by-n; MR = LOW; CF = HIGH; $\overline{CP1}$ = LOW.

PL	A3	A2	A1	A0	Divide by	TC output pulse width
L	X	X	X	X	16	one clock period
TC	H	H	H	H	15	clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	
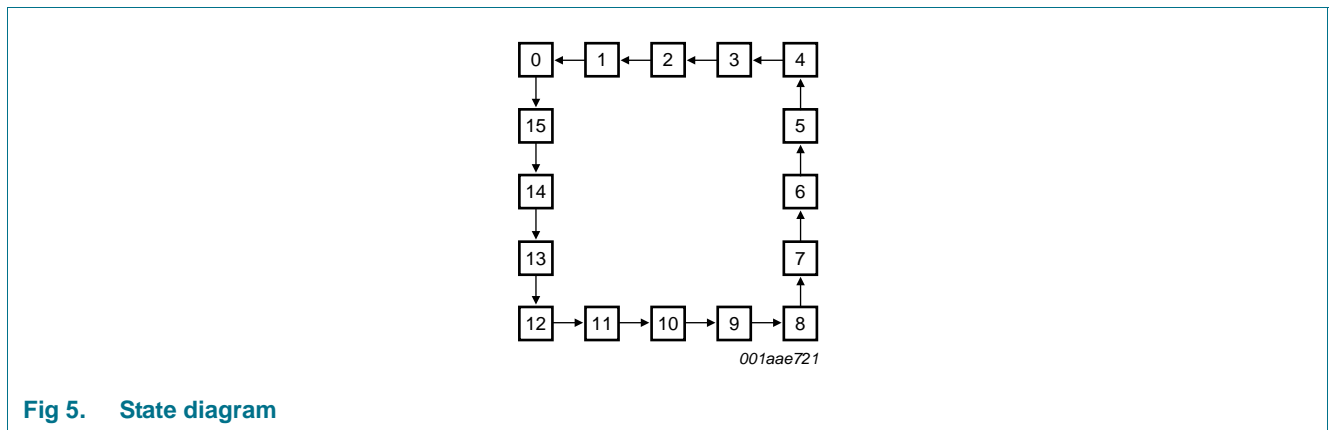
Fig 5. **State diagram**

7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current	to any supply terminal	-	±100	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
P_{tot}	total power dissipation	DIP16 package [1]	-	750	mW
		SO16 package [2]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 5$ V	-	-	3.75	µs/V
		$V_{CC} = 10$ V	-	-	0.5	µs/V
		$V_{CC} = 15$ V	-	-	0.08	µs/V

HEF4526B

Product data sheet **Rev. 5 — 22 November 2011** 7 of 19

9. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$|I_O|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$|I_O|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$|I_O|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$|I_O|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	−1.7	-	−1.4	-	−1.1	mA
		V_O = 4.6 V	5 V	-	−0.52	-	−0.44	-	−0.36	mA
		V_O = 9.5 V	10 V	-	−1.3	-	−1.1	-	−0.9	mA
		V_O = 13.5 V	15 V	-	−3.6	-	−3.0	-	−2.4	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 9.　Dynamic characteristics

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; for test circuit see Figure 7; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP0, $\overline{CP1}$ to Qn; see Figure 6	5 V	[1] 123 ns + (0.55 ns/pF)C_L	-	150	300	ns
			10 V	54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V	42 ns + (0.16 ns/pF)C_L	-	50	100	ns
		CP0, $\overline{CP1}$ to TC; see Figure 6	5 V	183 ns + (0.55 ns/pF)C_L	-	210	420	ns
			10 V	79 ns + (0.23 ns/pF)C_L	-	90	180	ns
			15 V	62 ns + (0.16 ns/pF)C_L	-	70	140	ns
		PL to Qn; see Figure 6	5 V	173 ns + (0.55 ns/pF)C_L	-	200	400	ns
			10 V	69 ns + (0.23 ns/pF)C_L	-	80	160	ns
			15 V	52 ns + (0.16 ns/pF)C_L	-	60	120	ns
		MR to Qn	5 V	113 ns + (0.55 ns/pF)C_L	-	140	280	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
t_{PLH}	LOW to HIGH propagation delay	CP0, $\overline{CP1}$ to Qn; see Figure 6	5 V	[1] 123 ns + (0.55 ns/pF)C_L	-	150	300	ns
			10 V	54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V	42 ns + (0.16 ns/pF)C_L	-	50	100	ns
		CP0, $\overline{CP1}$ to TC; see Figure 6	5 V	183 ns + (0.55 ns/pF)C_L	-	210	420	ns
			10 V	79 ns + (0.23 ns/pF)C_L	-	90	180	ns
			15 V	62 ns + (0.16 ns/pF)C_L	-	70	140	ns
		PL to Qn; see Figure 6	5 V	153 ns + (0.55 ns/pF)C_L	-	180	360	ns
			10 V	59 ns + (0.23 ns/pF)C_L	-	70	140	ns
			15 V	42 ns + (0.16 ns/pF)C_L	-	50	100	ns
t_t	transition time	see Figure 6	5 V	[1] 10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	An to PL; see Figure 6	5 V		30	0	-	ns
			10 V		20	0	-	ns
			15 V		15	0	-	ns
t_h	hold time	An to PL; see Figure 6	5 V		30	5	-	ns
			10 V		20	5	-	ns
			15 V		15	5	-	ns

HEF4526B

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet

Rev. 5 — 22 November 2011

9 of 19

Table 9.   Dynamic characteristics *…continued*

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; for test circuit see *Figure 7*; unless otherwise specified.

| Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_W	pulse width	CP0 input; LOW; see Figure 6	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
		$\overline{CP1}$ input; HIGH; see Figure 6	5 V		80	40	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
		PL input; HIGH; see Figure 6	5 V		100	50	-	ns
			10 V		40	20	-	ns
			15 V		32	16	-	ns
		MR input; LOW	5 V		130	65	-	ns
			10 V		50	25	-	ns
			15 V		40	20	-	ns
f_{max}	maximum frequency	PL = LOW; see Figure 6	5 V	[2]	6	12	-	MHz
			10 V		12	25	-	MHz
			15 V		16	32	-	MHz

[1]   The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2]   In the divide-by-n mode (PL connected to TC), the CP0 or $\overline{CP1}$ pulse width must be greater than the maximum HIGH to LOW propagation delay for CP0 or $\overline{CP1}$ to TC.

Table 10.   Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 10000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

HEF4526B

Product data sheet **Rev. 5 — 22 November 2011** **10 of 19**

11. Waveforms
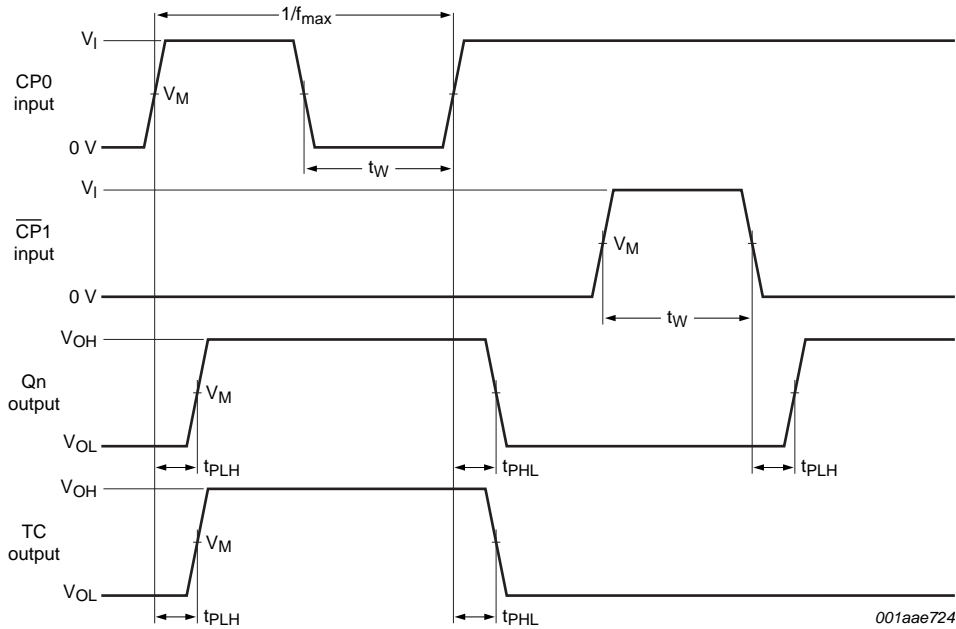
a. Propagation delays for CP0, $\overline{CP}1$ to Qn, and TC, minimum CP0 and $\overline{CP}1$ pulse widths and maximum frequency
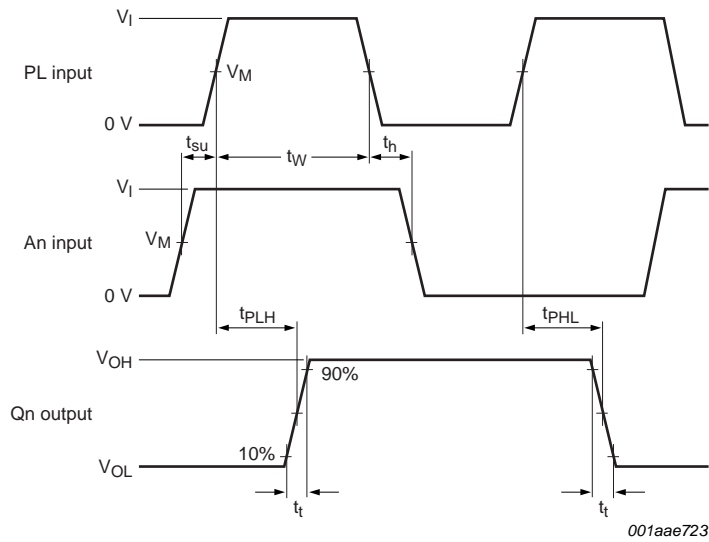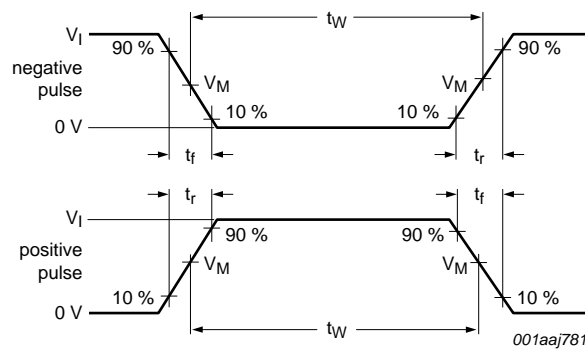
b. Propagation delays for PL and An to Qn, setup and hold times for PL to An, Qn transition times and minimum PL pulse width
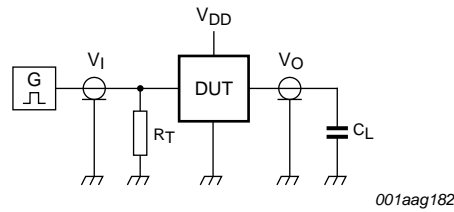
Measurement points are given in Table 11.

The logic levels V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Fig 6.   Waveforms showing switching times

HEF4526B

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet   **Rev. 5 — 22 November 2011**   11 of 19

a. Input waveforms

b. Test circuit

Test data is given in Table 11;

Definitions for test circuit:

DUT = Device Under Test;

C_L = Load capacitance, including jig and probe capacitance;

R_L = Load resistance;

R_T = Termination resistance, should be equal to the output impedance Z_o of the pulse generator.

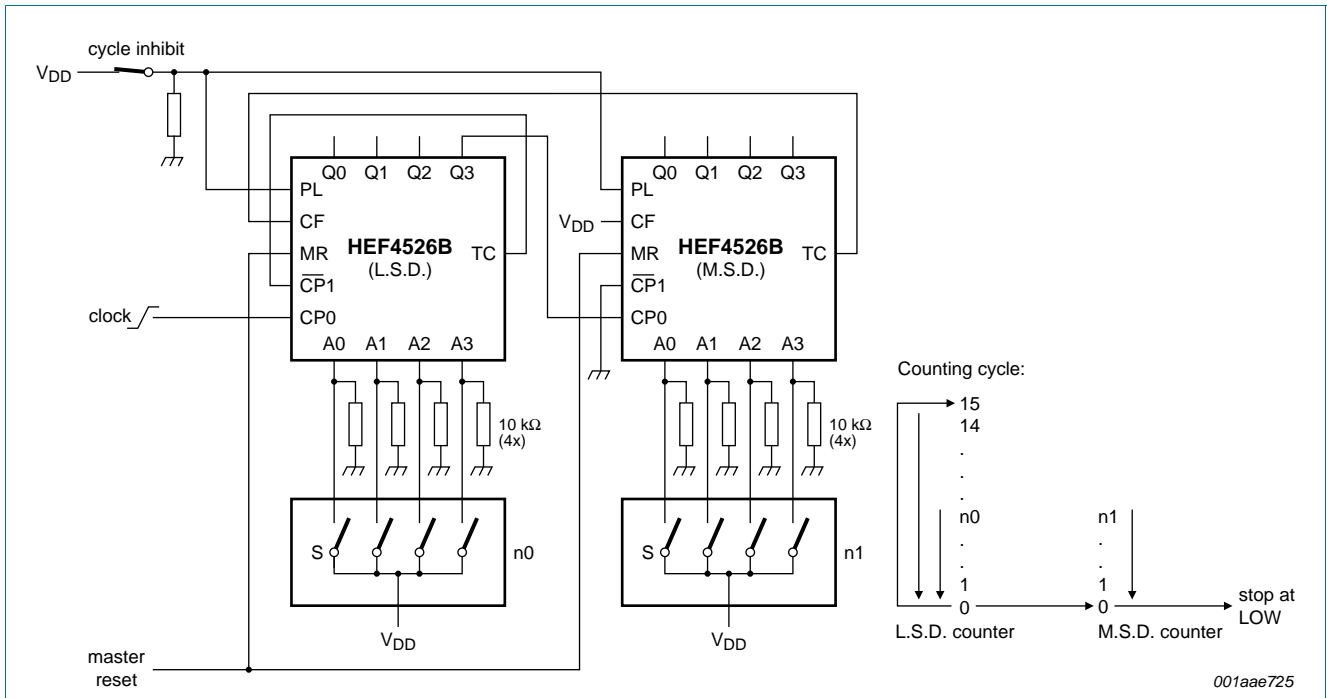**Fig 7.   Test circuit for switching times**

Table 11.   Measurement points and test data

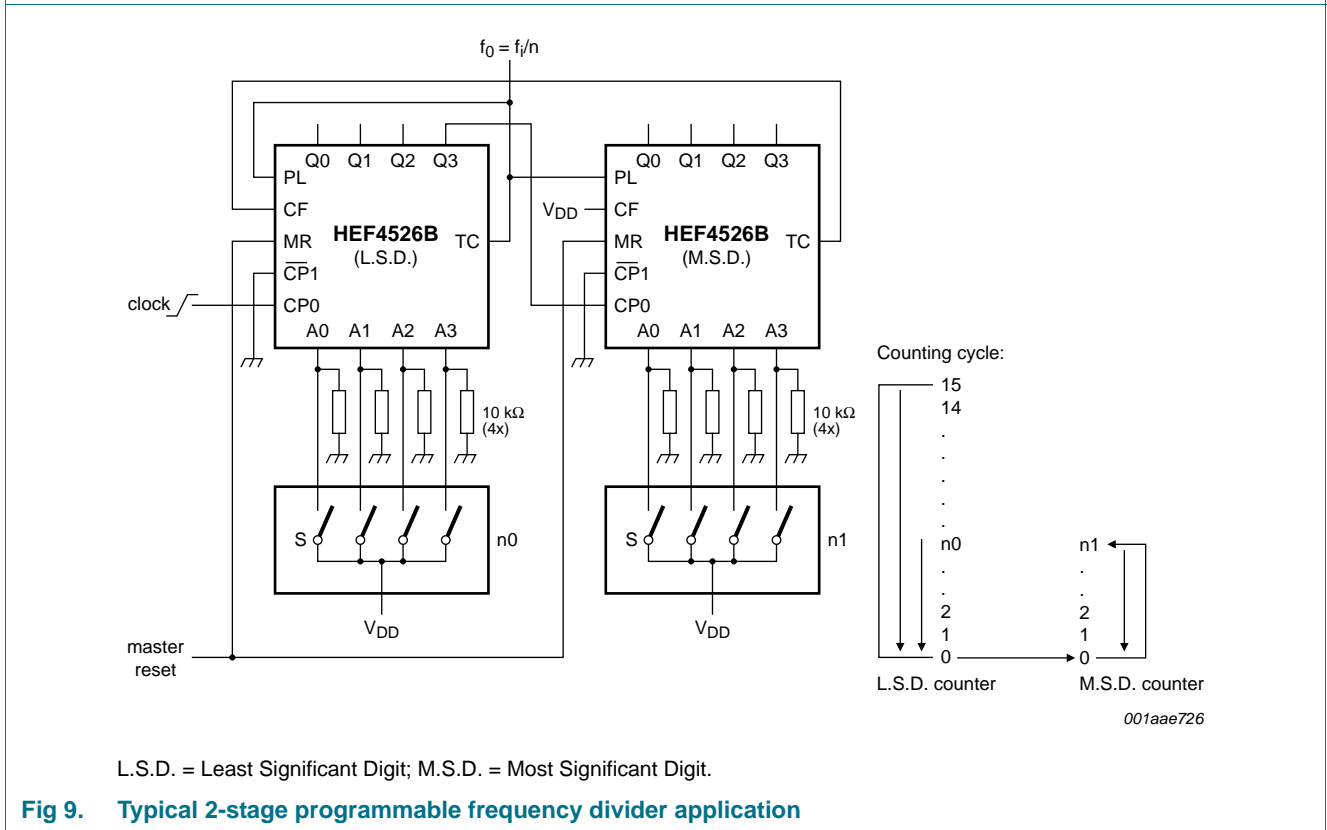| Supply voltage	Input			Load	
	V_I	V_M	t_r, t_f	C_L	R_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF	1 kΩ

12. Application information

Some examples of HEF4526B applications are:

- Divide-by-n counter
- Programmable frequency divider

L.S.D. = Least Significant Digit; M.S.D. = Most Significant Digit.

Fig 8.   **Typical 2-stage programmable down counter (one cycle) application.**

L.S.D. = Least Significant Digit; M.S.D. = Most Significant Digit.

Fig 9.   **Typical 2-stage programmable frequency divider application**

13. Package outline
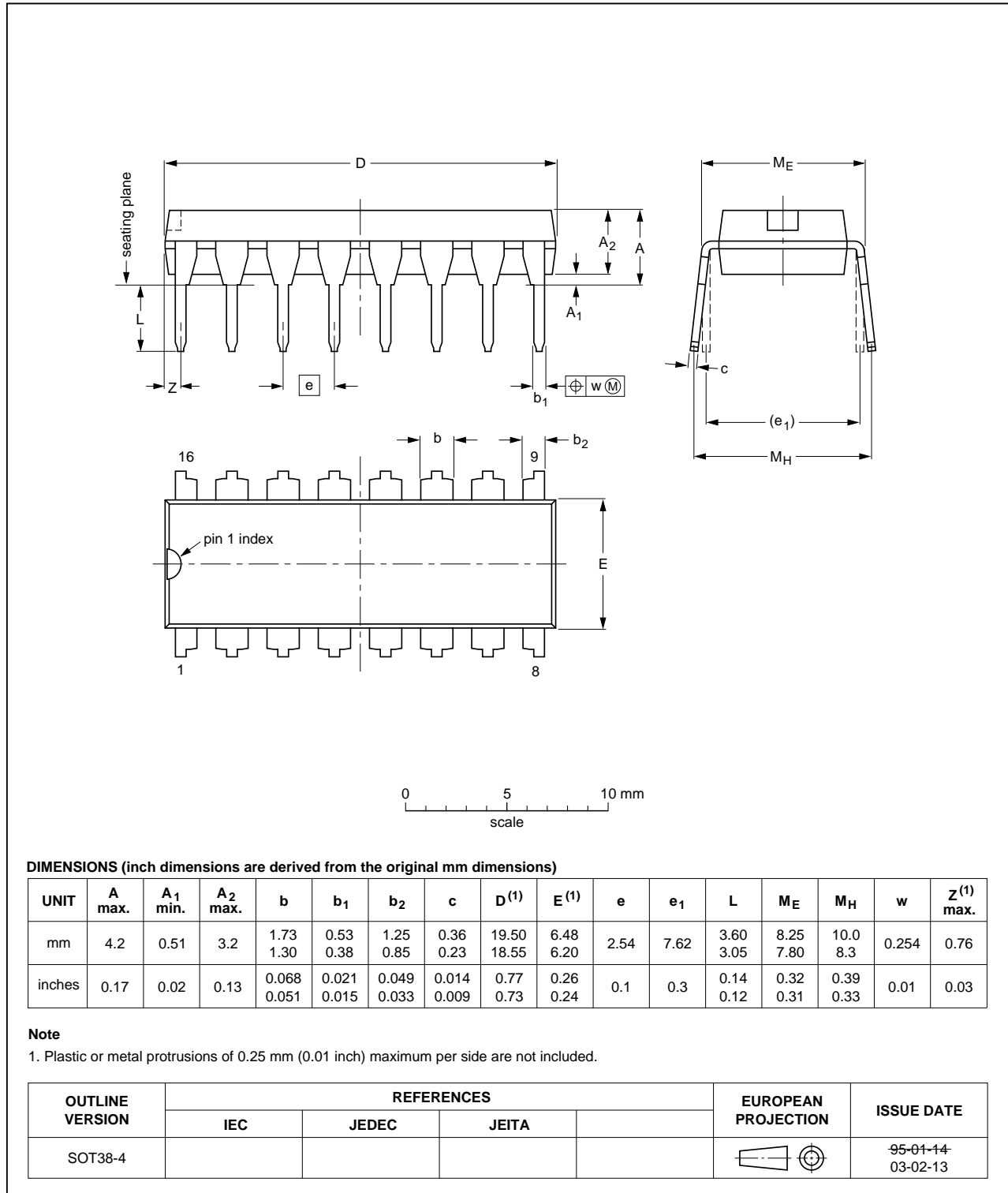
DIP16: plastic dual in-line package; 16 leads (300 mil)   **SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D[1]	E[1]	e	e₁	L	M_E	M_H	w	Z[1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 10. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

0   2.5   5 mm
scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D⁽¹⁾	E⁽¹⁾	e	H_E	L	Lₚ	Q	v	w	y	Z⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

HEF4526B

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet

Rev. 5 — 22 November 2011

15 of 19

14. Revision history

Table 12.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4526B v.5	20111122	Product data sheet	-	HEF4526B v.4
Modifications:	• Section Applications removed • Table 8: I_{OH} minimum values changed to maximum			
HEF4526B v.4	20090921	Product data sheet	-	HEF4526B_CNV v.3
HEF4526B_CNV v.3	19950101	Product specification	-	HEF4526B_CNV v.2
HEF4526B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HEF4526B

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet

Rev. 5 — 22 November 2011

17 of 19

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

HEF4526B

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Product data sheet

Rev. 5 — 22 November 2011

18 of 19

17. Contents

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP](#):
  [HEF4526BT,652](#) [HEF4526BT,653](#) [HEF4526BP,652](#)