

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC58** Dual AND-OR gate

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual AND-OR gate

74HC58

## FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC58 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The "58" provides two sections of AND-OR gates. One section contains a 2-wide, 3-input (1A to 1F) AND-OR gate and the second section contains a 2-wide, 2-input (2A to 2D) AND-OR gate.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 15\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
$t_{PHL}/t_{PLH}$	propagation delay	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$		
	1n to 1Y		11	ns
	2n to 2Y		9	ns
$C_I$	input capacitance		3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	18	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$

## ORDERING INFORMATION

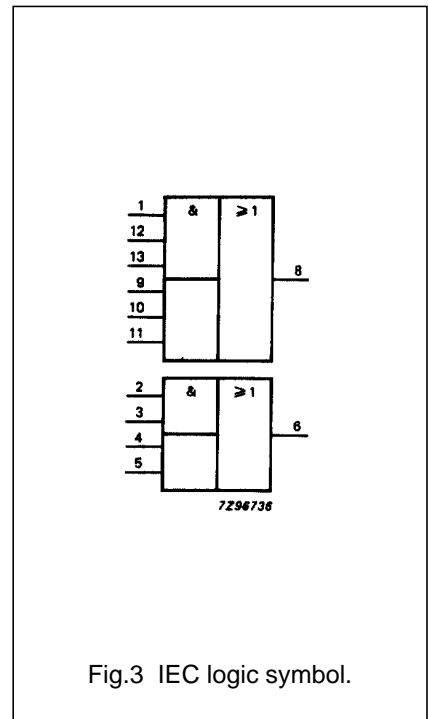
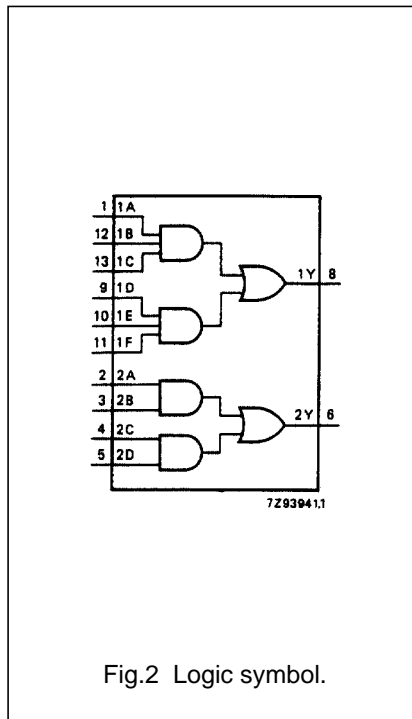
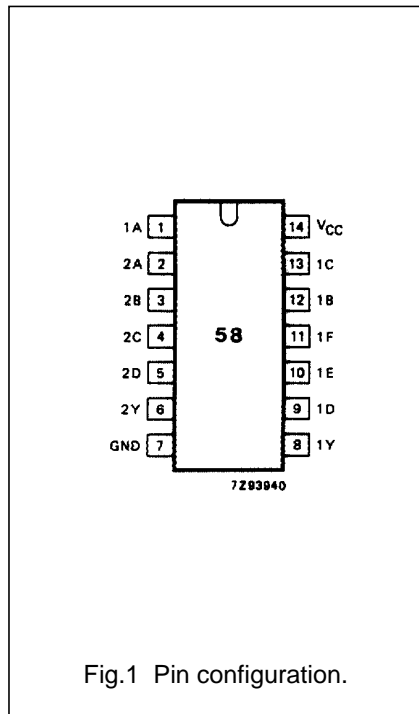
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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74HC58

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 12, 13, 9, 10, 11	1A to 1F	data inputs
2, 3, 4, 5	2A to 2D	data inputs
8, 6	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



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74HC58

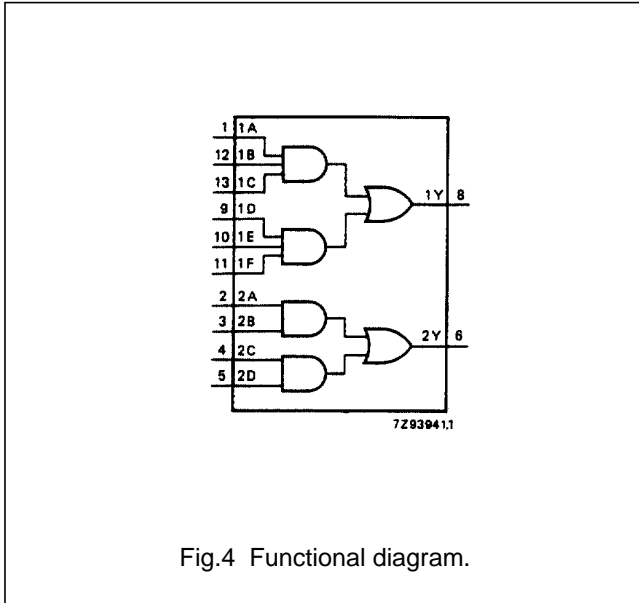


Fig.4 Functional diagram.

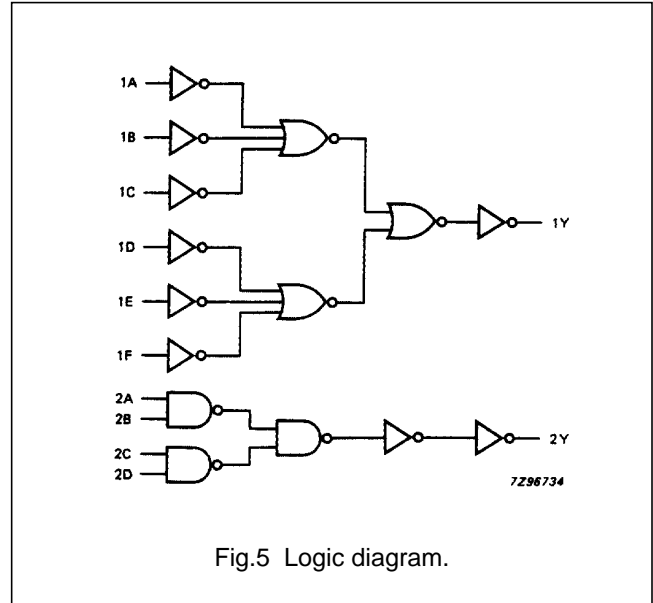


Fig.5 Logic diagram.

FUNCTION TABLE (1)

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
L	X	X	L	X	X	L
L	X	X	X	L	X	L
L	X	X	X	X	L	L
X	L	X	L	X	X	L
X	L	X	X	L	X	L
X	L	X	X	X	L	L
X	X	L	L	X	X	L
X	X	L	X	L	X	L
X	X	L	X	X	L	L
X	X	X	H	H	H	H
H	H	H	X	X	X	H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
L	X	L	X	L
L	X	X	L	L
X	L	L	X	L
X	L	X	L	L
X	X	H	H	H
H	H	X	X	H

Note

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

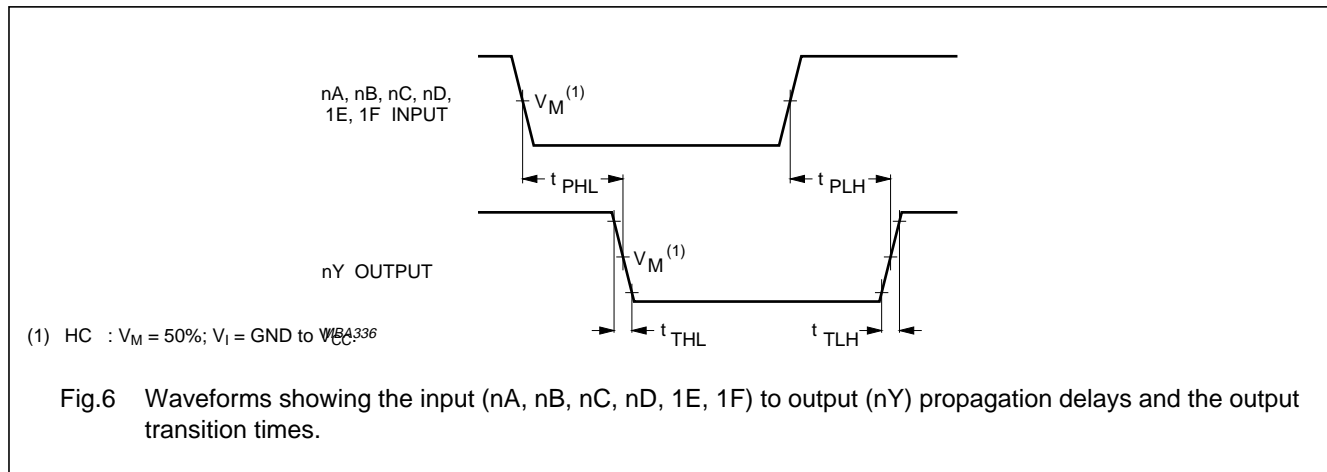
I<sub>CC</sub> category: SSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A,1B,1C,1D,1E, 1F to 1Y		36 13 10	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 2A,2B,2C,2D to 2Y		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

## AC WAVEFORMS



## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.